

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for transmitting data on a bus with minimization of ~~the~~ bus switching activity, the method comprising the steps of:

converting ~~the~~ a datum to be transmitted from its own original format into a transmission format that reduces the bus switching activity, said ~~step of~~ converting including: swapping ~~the~~ a position of one or more bits of the datum to be transmitted, said swapping being performable according to a plurality of different variants, each of which is identified by a respective sorting pattern; and selecting, between the ~~various~~ sorting patterns, a particular sorting pattern that reduces the bus switching activity upon transmission on the bus of the datum generated using said selected sorting pattern;

transmitting on the bus the datum in said transmission format; and transmitting on the bus the selected sorting pattern ~~(P)~~;

receiving the datum in said transmission format; and receiving the selected sorting pattern transmitted on the bus; and

converting the datum received from said transmission format to said original format using the selected sorting pattern received,

wherein a succession of said sorting patterns generated at a transmission end and a succession of sorting patterns generated at a reception end are synchronized with each using a common clock signal.

2. (Currently Amended) The method according to claim 1 wherein said ~~step of~~ transmitting on the bus the selected sorting pattern includes ~~comprises the steps of:~~

generating a said succession of sorting patterns identifying all ~~the~~ possible swaps of the position of the bit or bits of the datum to be transmitted;

comparing the ~~optimal~~particular sorting pattern to be transmitted with the sorting patterns generated; and

generating and transmitting on the bus a synchronization signal upon detection of the ~~an~~ identity between the ~~optimal~~particular sorting pattern to be transmitted and one of the sorting patterns generated .

3. (Currently Amended) The method according to claim 1-2 wherein said ~~step of~~ receiving the selected sorting pattern transmitted on the bus ~~includes~~comprises the steps of:

generating a ~~said~~ succession of sorting patterns identical to, and synchronous with, the ~~one~~-generated succession of sorting patterns identifying all possible swaps of the position of the bit or bits of the datum to be transmitted~~in transmission~~; and

identifying one of the succession of sorting patterns that is generated at the ~~an~~ instant of reception of the synchronization signal transmitted on the bus, the sorting pattern identified being identical to said selected sorting pattern to be transmitted.

4. (Currently Amended) The method according to claim 3 wherein the sorting pattern selected reduces the bus switching activity to a minimum amount ~~and the sorting pattern selected is the optimal sorting pattern.~~

5. (Currently Amended) The method according to claim 2, ~~characterized in that wherein~~ each of said steps of generating a ~~the~~ succession of sorting patterns includes ~~comprises the steps of~~:

providing a finite state machine having a number of internal states equal to ~~the~~ a number of possible swaps of the position of the bit or bits of the datum to be transmitted;

associating to each of the internal states of said finite state machine a respective sorting pattern; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate said sorting patterns.

6. (Currently Amended) The method according to claim 2, ~~characterized in that wherein each of said steps of generating a the~~ succession of sorting patterns ~~includes~~ comprises the step of:

generating a plurality of disjoint sets of sorting patterns, each set being formed by a sorting pattern identifying a respective subset of possible swaps of the position of the bit or bits of the datum to be transmitted, the sorting patterns of each set being further generated in succession and in a synchronous way with respect to the sorting patterns of the other sets.

7. (Currently Amended) The method according to claim 6, ~~characterized in that wherein the step of generating a the~~ plurality of separate sets of sorting patterns ~~comprises~~ includes, for each said set of sorting patterns, ~~the steps of~~:

providing a finite state machine having a number of internal states equal to ~~the a~~ number of sorting patterns in the set;

associating to each of the internal states of said finite state machine a respective sorting pattern; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate the corresponding sorting patterns.

8. (Currently Amended) A ~~device~~ system for transmitting data on a bus with minimization of ~~the~~ bus switching activity, the device comprising:

first converting means for converting ~~the a~~ datum to be transmitted from its own original format ~~($b(t)$)~~ to a transmission format ~~($B(t)$)~~ that minimizes the bus switching activity, said first converter means ~~comprising~~ including:

a swap operator for swapping ~~the a~~ position of one or more bits of the datum to be transmitted, said swapping being performable according to a plurality of different variants, each of which is identified by a respective sorting pattern ~~(P_i)~~; and

selecting means for selecting, between the various sorting patterns, an optimal sorting pattern ~~(P_i)~~ that minimizes the bus switching activity upon transmission on the bus of the datum generated using said optimal sorting pattern ~~(P_i)~~;

~~said transmission device further comprising:~~

transmitting means for transmitting on the bus the datum in said transmission format ~~($B(t)$)~~ and the optimal sorting pattern ~~(P_t)~~;

receiving means for receiving the datum in said transmission format ~~($B(t)$)~~ and said optimal sorting pattern ~~(P_t)~~ transmitted on the bus; and

second converting means for converting the datum received from said transmission format ~~($B(t)$)~~ to said original format ($b(t)$) using said optimal sorting pattern ~~(P_t)~~ received,

~~said transmission device being characterized in that~~wherein said transmitting means ~~comprise~~includes:

first sorting pattern generating means for generating a succession of sorting patterns identifying all ~~the~~ possible swaps of the position of the bit or bits of the datum to be transmitted;

comparing means for comparing the optimal sorting pattern ~~(P_t)~~ to be transmitted with the sorting patterns generated;

signal generating means for generating and sending onto said bus a synchronization signal ~~(S_{yne})~~ upon detection of ~~the~~ an identity between the optimal sorting pattern ~~(P_t)~~ to be transmitted and one of the sorting patterns generated,

~~said transmission device being further characterized in that~~wherein said receiving means ~~comprise~~includes:

second sorting pattern generating means for generating a succession of sorting patterns identical to, and synchronous with, the ~~one~~ sorting patterns generated ~~in transmission~~by said first sorting pattern generating means; and

detecting means for identifying one of the sorting patterns generated by said second sorting pattern generating means at ~~the~~ an instant of reception of the synchronization signal ~~(S_{yne})~~ transmitted on the bus, the sorting pattern identified being identical to said optimal sorting pattern ~~(P_t)~~ to be transmitted,

wherein said succession of said sorting patterns generated at transmission and said succession of sorting patterns generated at reception are synchronized with each using a common clock signal.

9. (Currently Amended) The ~~device~~-system according to claim 8, ~~characterized in that~~ wherein said first and second sorting pattern generating means each ~~comprise~~-include a finite state machine having a number of internal states equal to ~~the~~-a number of possible swaps of the position of the bit or bits of the datum to be transmitted, a respective sorting pattern being associated to each of the internal states of said finite state machine, said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate said sorting patterns.

10. (Currently Amended) The ~~device~~-system according to claim 8, ~~characterized in that~~ wherein said first and second sorting pattern generating means each ~~comprise~~-include a plurality of sorting pattern modules generating a plurality of disjoint sets of sorting patterns, each set being formed by a sorting pattern identifying a respective subset of all the possible swaps of the position of the bit or bits of the datum to be transmitted, the sorting patterns of each set being further generated in succession and in a synchronous way with respect to the sorting patterns of ~~the~~-other sets.

11. (Currently Amended) The ~~device~~-system according to claim 10, ~~characterized in that~~ wherein each of said sorting pattern generating modules comprises a finite state machine having a number of internal states equal to ~~the~~-a number of sorting patterns of the corresponding set, a respective sorting pattern being associated to each of the internal states of said finite state machine, said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate said sorting patterns.

12. (Currently Amended) A computer product loadable into ~~the~~-a memory of ~~a processor~~-associated with a bus, said computer product ~~comprising~~-having portions of software

~~code that can implement the method according to claim 8 when the computer product is run on a digital processor associated to the bus~~ are executable by a processor to minimize bus switching activity, by:

converting a datum to be transmitted from its own original format into a transmission format that reduces the bus switching activity, said converting including: swapping a position of one or more bits of the datum to be transmitted, said swapping being performable according to a plurality of different variants, each of which is identified by a respective sorting pattern; and selecting, between the sorting patterns, a particular sorting pattern that reduces the bus switching activity upon transmission on the bus of the datum generated using said selected sorting pattern;

transmitting on the bus the datum in said transmission format; and

transmitting on the bus a synchronization signal usable by a receiving device to identify said selected sorting pattern from a plurality of sorting patterns,

wherein a succession of said sorting patterns generated at a transmission end and a succession of sorting patterns generated at a reception end are synchronized with each using a common clock signal.

13. (Currently Amended) A method for ~~transmitting~~ communicating n -bit data on a single line, ~~characterized in that the transmission of a datum comprises the steps of~~ comprising:

in transmission:

generating in succession all the possible combinations of n bits;

comparing ~~the~~ an n -bit datum to be transmitted with the combinations of n bits generated; and

generating and transmitting on ~~a~~ said single line an identity signal upon detection of ~~the~~ a coincidence between the n -bit datum to be transmitted and one of the combinations of n bits generated, and

and in that the reception of the datum transmitted comprises the steps of

reception:

generating a succession of combinations of n bits identical and synchronous to the one-combinations generated in succession in transmission and synchronous with respect to the latter; and

identifying one of the combination of n bits generated at the an instant of reception of the identity signal transmitted on the single line, the combination of n bits identified being identical corresponding to the n -bit datum to be transmitted, wherein said succession of combinations generated at transmission and said succession of combinations generated at reception are synchronized with each using a common clock signal.

14. (Currently Amended) The method according to claim 13, ~~characterized in that~~ wherein said steps of generating in succession all the possible combinations of n bits in said transmission and in said reception comprises the steps of includes:

providing a finite state machine having a number of internal states equal to ~~the a~~ number of possible combinations of n bits;

associating to each of the internal states of said finite state machine a respective combination of n bits; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of n bits.

15. (Currently Amended) The method according to claim 13, ~~characterized in that~~ wherein said steps of generating the combinations of n bits in said transmission and in said reception comprises the steps of includes:

generating a plurality of disjoint sets of possible combinations of n bits, the combinations of n bits of each set being further generated in succession and in a synchronous way with respect to the combinations of n bits of the other sets.

16. (Currently Amended) The method according to claim 15, ~~characterized in that~~ wherein the step of generating a plurality of disjoint sets of possible combinations of n bits

in said transmission and in said reception comprisesincludes, for each said set of combinations of n bits,~~the steps of:~~

providing a finite state machine having a number of internal states equal to ~~the a~~ number of combinations of n bits in the set;

associating to each of the internal states of said finite state machine a respective combination of n bits; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of n bits.

17. (Currently Amended) A ~~device-system~~ for transmitting n -bit data on a single line, ~~characterized in that it comprises~~comprising:

at ~~the a~~ transmission end:

first combination generating means for generating in succession all ~~the~~ possible combinations of n bits;

comparing means for comparing ~~the an~~ n -bit datum to be transmitted with the combinations of n bits generated; and

signal generating means for generating and transmitting on a-said single line an identity signal upon detection of ~~the a~~ coincidence between the n -bit datum to be transmitted and one of the combinations of n bits generated; and
~~and in that it comprises,~~ at ~~the a~~ reception end:

second combination generating means for generating ~~the a~~ same succession of combinations of n bits as that generated by the first combination generating means, the successions of combinations of n bits generated by the said first and second combination-generating means being synchronized with one another; and

detecting means for identifying one of the combination of n bits generated by said second combination generating means at ~~the an~~ instant of reception of the identity signal transmitted on the single line, the combination of n bits identified ~~being identical~~corresponding to the n -bit datum to be transmitted,

wherein said succession of combinations generated at said transmission end and said succession of combinations generated at said reception end are synchronized with each using a common clock signal.

18. (Currently Amended) The ~~device~~-system according to claim 17, ~~characterized in that~~ wherein each of said first and second combination generating means ~~comprises-include~~ a finite state machine having a number of internal states equal to ~~the~~-a number of possible combinations of n bits, a respective combination of n bits being associated to each of the internal states of said finite state machine, and said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of n bits.

19. (Currently Amended) The ~~device~~-system according to claim 17, ~~characterized in that~~ wherein said first and second combination generating means each ~~comprise~~ include a plurality of combination generating modules generating a plurality of disjoint sets of possible combinations of n bits, the combinations of n bits of each set being generated in succession and in a synchronous way with respect to the combinations of n bits of the other sets.

20. (Currently Amended) The ~~device~~-system according to claim 19, ~~characterized in that~~ wherein each of said combination generating modules ~~comprises-include~~s a finite state machine having a number of internal states equal to ~~the~~-a number of combinations of n bits in the set, a respective combination of n bits being associated to each of the internal states of said finite state machine, and said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of n bits.

21. (Currently Amended) A computer product loadable into ~~the~~-a memory of ~~a processor associated with a bus~~, said computer product ~~comprising-including~~ portions of software code that can implement the method according to claim 13 when the computer product is ~~run on~~executed by a digital processor associated to the bus.

22. (New) A transmitter device, comprising:

a converter to convert a datum to be transmitted from an initial format to a transmission format, said transmission format being a selected sorting pattern from among a succession of sorting patterns that identify possible swaps of bit positions of said datum;

a first finite state machine having a number of internal states equal to a number of said sorting patterns and each of said internal states respectively corresponding to one of said sorting patterns; and

a common clock adapted coupled to said first finite state machine to synchronize said first finite state machine with a second finite state machine, at a receiving end, that receives said datum in said transmission format and that also has a number of internal states equal to said number of said sorting patterns and each of said internal states of said second finite state machine at the receiving end also respectively corresponding to one of said sorting patterns,

wherein said first finite state machine is adapted to generate a synchronization signal to be received by said second state machine, said synchronization signal corresponding to a particular state of said first finite state machine and adapted to be used by said second finite state machine to identify said selected sorting pattern.

23. (New) The device of claim 22, further comprising a register to store said sorting patterns.

24. (New) The device of claim 22 wherein said sorting patterns are from among a plurality of disjoint sets of sorting patterns.